[0049] What is claimed is:

1. A system comprising:

at least two processing units embedded on a chip able to communicate with each other and to generally independently control access to data from memory on said chip.

2. A system according to claim 1 and further comprising at least one first in first out (FIFO) unit used by said processing units to transfer data therebetween.

3. A system according to claim 2 and further comprising a data flow control unit able to control data transfer.

4. A system according to claim 1 wherein said processing units are central processing units (CPUs).

5. A system according to claim 1 and further comprising at least two asynchronous clocks controlling said at least two processing units.

6. A system according to claim 1 wherein one of said processing units is able to process media access control (MAC) commands and another of said processing units is able to process physical layer device (PHY) commands of a networking protocol.

7. A system comprising:

at least two CPUs embedded on a chip able to communicate with each other and to asynchronously control reading and writing of data to and from memory on said chip.

8. A system according to claim 7 and further comprising at least one FIFO unit used by said CPUs to transfer data therebetween.

9. A system according to claim 7 and further comprising a control unit to control data transfer.

10. A system according to claim 7 and further comprising at least two asynchronous clocks controlling said at least two CPUs.

11. A system according to claim 7 wherein one of said CPUs is able to process MAC commands and another of said CPUs is able to process PHY commands of a networking protocol.

12. A system comprising:

at least two processing units embedded on a chip able to asynchronously transfer data therebetween.

13. A system according to claim 12 wherein said processing units are CPUs.

14. A system according to claim 12 and further comprising at least one FIFO unit used by said processing units to transfer data therebetween.

15. A system according to claim 14 and further comprising a control unit to control data transfer.

16. A system according to claim 12 wherein one of said processing units is able to process MAC commands and another of said processing units is able to process PHY commands of a networking protocol.

17. An apparatus comprising:

a FIFO unit able to receive data from a first random access memory (RAM) accessible by a first CPU embedded on a chip and able to write said data to a second RAM accessible by a second CPU embedded on said chip.

18. An apparatus according to claim 17, further comprising at least one control unit able to control data flow to and from said FIFO unit.

19. An apparatus according to claim 18 wherein said at least one control unit is a direct memory access unit (DMA).

20. An apparatus according to claim 18, wherein said at least one control unit comprises at least one read channel able to control receipt of said data.

21. An apparatus according to claim 18, wherein said at least one control unit comprises at least one write channel able to control transmission of said data.

22. An apparatus according to claim 17, further comprising a register accessible by said first CPU and said second CPU.

23. An apparatus according to claim 17 wherein said first CPU is able to process MAC commands and said second CPU is able to process PHY commands of a networking protocol.

24. A chip having a FIFO unit, a first memory, a second memory, a first processing unit, and a second processing unit all embedded thereon wherein said FIFO unit is able to receive data from said first memory accessible by said first processing unit and able to write said data to said second memory accessible by said second processing unit.

25. A chip according to claim 24 wherein said first processing unit and said second processing unit are CPUs.

26. A chip according to claim 24 wherein said first memory and said second memory are RAM.

27. A chip according to claim 24 and further comprising a register accessible by said first processing unit and said second processing unit.

28. A system comprising: